CLAIMS

1.

A permanently-ON MOS transistor (21) comprising:

a silicon source region (9') of a first conductivity type;

a silicon drain region (9') of the first conductivity type;

a silicon well region (3) of a second conductivity type, in which said source region and drain region are buried;

a silicon contact region (15) of the first conductivity type, buried in the well region (3), said contact region (15) contacting said source region (9') and said drain region (9');

a first gate insulating layer (2) selectively placed over the silicon source region (9') and the silicon drain region (9');

a second gate insulating layer (7) selectively placed over the first gate insulating layer (2) and over the silicon contact region (15); and

a polysilicon gate region (8') placed over the second gate insulating layer (7).

2.

The MOS transistor of claim 1, wherein said first conductivity type is a P conductivity type and said second conductivity type is a N conductivity type.

3.

The MOS transistor of claim 1, wherein said first conductivity type is a N conductivity type and said first conductivity type is a P conductivity type.

4.

The MOS transistor of claim 1, wherein said first gate insulating layer is a first gate oxide layer and said second gate insulating layer is a second gate oxide layer.

5.

An EEPROM circuit comprising the permanently ON MOS transistor of claim 1.

6.

An integrated circuit structure for MOS-type devices comprising at least one permanently-ON MOS transistor (21), said transistor including:

a first silicon source region (9′) of a first conductivity type;

a first silicon drain region (9′) of the first conductivity type;

a first silicon well region (3) of a second conductivity type, in which the first silicon source region (9′) and the first silicon drain region (9′) are buried;

a silicon contact region (15) of the first conductivity type, buried in the well region (3), the contact region (15) contacting the silicon source region (9′) and the silicon drain region (9′);

a first gate insulating layer (2) selectively placed over the silicon source region (9′) and the silicon drain region (9′);

a second gate insulating layer (7) selectively placed over the first gate insulating layer (2) and over the silicon contact region (15); and

a first polysilicon gate region (8′) placed over the second gate insulating layer (7).

7.

The circuit structure of claim 6, further comprising at least one non-permanently-ON MOS transistor (23), said at least one non-permanently-ON transistor including:

a second silicon source region (9″) of the first conductivity type;

a second silicon drain region (9″) of the first conductivity type:

a second silicon well region (3) of a second conductivity type, in which said second source region and said second drain region are buried, said second silicon well region (3) being said first silicon well region (3); and

a second polysilicon gate region (8″),

wherein:

said first gate insulating layer (2) is placed over said second silicon source region (9″) and over said second silicon drain region (9″);

said second gate insulating layer (7) is placed over said first gate insulating layer (2); and

said second polysilicon gate region (8″) is placed over said second gate insulating layer.

8.

The integrated circuit structure of claim 6, wherein said first conductivity type is a P conductivity type and said second conductivity type is a N conductivity type.

9.

The integrated circuit structure of claim 6, wherein said first conductivity type is a N conductivity type and said first conductivity type is a P conductivity type.

10.

The integrated circuit structure of claim 6, wherein said first gate insulating layer is a first gate oxide layer and said second gate insulating layer is a second gate oxide layer.

11.

An EEPROM circuit comprising the integrated circuit structure of claim 6.

12.

A process for forming a permanently-ON MOS transistor (21) comprising the steps of:

providing a silicon well region (3) of a first conductivity type;

depositing a first insulating layer (2) over the silicon well region (3) of the first conductivity type;

removing a portion of said deposited first insulating layer;

forming a buried silicon region (15) of a second conductivity type within the silicon well region (3) of the first conductivity type, under the removed portion of said deposited first insulating layer;

depositing a second insulating layer (7) over the first insulating layer (2) and over the buried silicon region (15) of the second conductivity type;

forming a polysilicon gate region (8′) over the second insulating layer; and

forming a source region (9′) of the second conductivity type and a drain region

(9') of the second conductivity type within the buried silicon well region (3), said source region and drain region contacting said buried silicon region (15) of the second conductivity type.

13.

The process according to claim 12, wherein said step of forming a source region (9') of the second conductivity type and a drain region (9') of the second conductivity type within the buried silicon well region (3) is the last step in time of the steps of claim 4.

14.

The process of claim 12, wherein said first conductivity type is a P conductivity type and said second conductivity type is a N conductivity type.

15.

The process of claim 12, wherein said first conductivity type is a N conductivity type and said first conductivity type is a P conductivity type.

16.

The process of claim 12, wherein said first gate insulating layer is a first gate oxide layer and said second gate insulating layer is a second gate oxide layer.

17.

The process of claim 12, wherein said permanently ON transistor makes part of an EEPROM circuit.